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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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THOMAS, KAYDEN, HOSTEMEYER & RISLEY LLP
100 GALLERIA PARKWAY
SUITE 1750
ATLANTA, GA 30339

EXAMINER	
AHMADI, MOHSEN	
ART UNIT	**PAPER NUMBER**
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/798,558	LU ET AL.
	Examiner	Art Unit
	Mohsen Ahmadi	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *10-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/06/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (US Pat. 20030049938) in view of Broermann et al. (US Pat. 20040201858) and Kota et al. (US Pat. 20050148104).

The present claim generally requires a method for forming a calibrated critical dimension test wafer for process control of sub-tenth micron polysilicon features comprising: providing a wafer substrate, forming a pad oxide on wafer substrate, depositing a metal layer on pad oxide, patterning metal layer to form at least one metal plate in at least one region of wafer substrate, milling a plurality of substantially parallel trenches in at least one metal plate with a focused ion beam, thereby forming a critical dimension test array and measuring the widths of parallel trenches and the spacing therebetween, thereby calibrating dimension test array.

Regarding claim 1, Lai et al. discloses a silicon wafer comprising a first level interlayer dielectric (is grown on the wafer by flowing oxygen in a process chamber to react with silicon thus producing a silicon dioxide) (See page. 1 paragraph [0005]), depositing a metal layer such as aluminum on the first level interlayer dielectric (silicon

dioxide), patterning the metal layer to form metal lines on the wafer substrate (See page. 1 paragraph [0004]). Lai et al. also discloses trenches in the device (See page. 1 paragraph [0007-0021]). Lai et al. also discloses focused ion beam (FIB) for examining, analyzing and repairing processing layers where these ions are focused by a lens into a small precise area that impacts the wafer (See page.1 paragraph [0027]).

Lai et al. discloses all of the claimed features as stated above except for forming a critical dimension test array and measuring the widths of parallel trenches and the spacing therebetween, thereby calibrating critical dimension test array.

Regarding claim 1, Broermann et al. discloses a method for measuring a characteristic dimension of at least one pattern on a disc-shaped object in a measuring instrument. Broermann et al. also discloses that the widths and the spacing of trenches can be examined in the CD measurement (See page. 3 paragraph [0025]).

Regarding claim 1, Kota et al. discloses a process controls for improved wafer uniformity using integrated or standalone metrology. Kota et al. also discloses, in order to control processing steps during semiconductor processing it is necessary to remove one or more test wafers from processing cluster for either destructive or non-destructive measurement (See page. 1 paragraph [0006]).

It would have been obvious to one of ordinary skill in the art, at the time of invention to use the critical dimension test array of Kota et al. and measuring the widths of parallel trenches and the spacing therebetween of Broermann et al. in the process of Lai et al. for it's known benefit making cross-sections and specific locations of the wafer.

Regarding claims 2, Lai et al. discloses producing a silicon dioxide that is grown on the wafer by flowing oxygen in a process chamber to react with silicon (See page. 1 paragraph [0005]). The examiner makes note that Lai et al. does not explicitly state a thickness of between 50-200 nm. However the examiner takes the position that the choice of range is not critical to the method of the invention; therefore, the range is a matter of choice. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to optimize the thickness of pad oxide layer of Lai et al. and arrive at the claimed thicknesses. This accords with the rule that discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art. *In re Antoine* , 195 USPQ 6, (CCPA 1977). The amount of metal layer thickness of Lai et al. is a matter of optimization and would be obvious to one of ordinary skill in the art.

Regarding claims 3, Lai et al. discloses a metal layer such as aluminum alloy (See page. 1 paragraph [0004]). The examiner makes note that Lai et al. does not explicitly state a thickness of between 400-1000 nm. However the examiner takes the position that the choice of range is not critical to the method of the invention; therefore, the range is a matter of choice. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to optimize the thickness of metal layer of Lai et al. and arrive at the claimed thicknesses. This accords with the rule that discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art. *In re Antoine* , 195 USPQ 6, (CCPA 1977). The amount of metal layer

thickness of Lai et al. is a matter of optimization and would be obvious to one of ordinary skill in the art.

Regarding claims 4, Lai et al. discloses where the metal layer is an alloy of aluminum and copper (See page. 1 paragraph [0003]).

Regarding claims 7 and 8, Lai et al. relied upon as discussed above and disclose all of the claimed features as stated above except for the trenches are between about 30 and 90 nm wide and have a width uniformity 3-sigma of between about 3.0 and 3.5 nm and mean value of width roughness of between about 3.0 and 3.7 nm and a mean value of edge roughness of between about 1.8 and 2.2 nm.

Broermann et al. discloses the parameter of the CD measurement P4 (See figure. 2) can be uniquely related to the 3-sigma. Broermann et al. also discloses a deviations from the mean value calculated from the repeated CD measurements on the one pattern (See page. 3 paragraph [0027 and 0030]). Broermann et al. also discloses the spacing, as well as the length and width of trenches, can be examined in the CD measurement (See page. 3 paragraph [0025]).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to optimize the trenches thickness, width uniformity, mean value of width roughness and a mean value of edge roughness of Lai et al. in light of the disclosure of Broermann et al. and arrive at the claimed thicknesses, width uniformity, mean value of width roughness and a mean value of edge roughness. This accords with the rule that

discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art. *In re Antoine* , 195 USPQ 6, (CCPA 1977). The amount of metal layer thickness of Lai et al. and Broermann et al. is a matter of optimization and would be obvious to one of ordinary skill in the art.

Regarding claim 9, Lai et al. discloses a scanning electron microscope (SEM) has been used for measurements (See page. 3 paragraph [0026]).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (US Pat. 20030049938) in view of Broermann et al. (US Pat. 20040201858) and Kota et al. (US Pat. 20050148104) and further in view of Wieczorek et al. (US Pat. 20040121531).

Regarding claims 5 and 6, Lai et al., Broermann et al. and Kota et al. are relied upon as discussed above and disclose all of the claimed features as stated above except for the ions are germanium and ion beam has an energy of between about 25 and 35 keV and a current of between about 0.5 and 3pA.

Regarding claims 5 and 6, Wieczorek et al. discloses a method of removing features using an improved removal process in the fabrication of a semiconductor device. Wieczorek et al. also discloses where ions are germanium and ion beam has energy and a current. Wieczorek et al. discloses semiconductor ions, for example, silicon or germanium, may be employed. Wieczorek et al. also discloses where the appropriate ion energy is in the range of approximately 10-80 KeV (See page. 4 paragraph [0048]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the germanium and energy of between about 25 and 35 KeV of ion beam of Wieczorek et al. in the process of Lai et al., Broermann et al. and Kota et al. for it's known benefit concurrently modifying the band structure of the implant regions on the device, for example, to reduce the substrate floating effect in SOI MOSFETs. In addition, the irradiation of ions also improves the etching of the silicon oxide layer.

Allowable Subject Matter

Claims 10-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The cited prior art does not disclose or suggest providing a calibrated critical dimension test wafer having a plurality of substantially parallel trenches milled, with a focused ion beam, in a metal plate formed over a pad oxide, and calibrated according to the process cited by claim 1; mounting and inserting said calibrated critical dimension test wafer in the sample chamber of a process control scanning electron microscope; calibrating process control scanning electron microscope by measuring the widths of trenches and the spaces therebetween and after calibrating, using process control scanning electron microscope to measure widths and spacing of polysilicon lines on an in-process integrated circuit wafer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsen Ahmadi whose telephone number is 1-571-272-5062. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 1-571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MA

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER